3.4 Gate Work Function Engineering for Nanotube-Based Circuits

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New nano-materials, such as single-wall carbon nanotubes (CNs), are considered a possible solution for future nano-electronics. The combination of ballistic transport, high carrier velocity, and ultra-thin body plus the intrinsic availability of matched n- and p-FETs make CNs an attractive candidate for high-speed and low-power logic applications.

A state-of-the-art CNFET consists of an undoped semiconducting CN channel in direct contact with source/drain (S/D) electrodes and a gate overlapping the entire channel to ensure proper switching of the device, called a Schottky barrier (SB) CNFET. In such a structure the threshold voltage V_{th} is controlled by the SB height, the CN diameter (t_{NT}), the gate oxide thickness (t_{ox}) and the metal gate work function (Φ_{WF}). $t_{NT,}$ which is inversely proportional to the energy gap (E_g) of the nanotube, impacts V_{th} directly as discussed in a previous publication [1].

Figure 3.4.1 shows simulated characteristics for a CNFET with E_g=0.9eV and a gate dielectric of 2nm SiO_2. A non-equilibrium Green's function (NEGF) approach is used [2]. As illustrated in the band diagrams, the switching of the CNFET is mainly due to the change of the SB by the gate voltage. Because of this, an inverse subthreshold slope larger than 60mV/dec is usually observed and becomes progressively larger with increasing $t_{ox,}$ which results in a scaling of V_{th}. The ambipolar characteristics of the CNFET provide a pair of p- and n- branches which can be used in principle for CMOS architecture, however, the leakage branch of one type of characteristics always has a similar current level as the main branch (on-current) of the other. Therefore, obtaining control of V_{th} in an ambipolar device is not only important to realize the desired supply voltage (V_{dd}), but also critical to achieve a pair of p- and n-type characteristics which are suitable for CMOS logic. With this perspective in mind, a study on the Φ_{WF} impact on CN-based circuits is presented here.

For a given undoped CNFET with a fixed SB-height, E_g and t_{ox}, the gate metal is the only way to control V_{th}. The inset of Fig. 3.4.2 shows a pair of FETs fabricated on the same CN, with two different metal gates, palladium (Pd) and aluminum (Al). The CN is located on a heavily p- doped Si substrate with 100nm SiO_2. Three Pd electrodes (200nm wide with 500nm spacing) are shared as S/D between the two FETs. 12nm of Al_2O_3 is deposited as the gate dielectric, prior to the Pd or Al gate definition on top of the FET. The CNs used here have diameters of ~2nm. Despite the fact that the rather large t_{NT} is responsible for a non-ideal on/off ratio, compared with Fig. 3.4.1, the leakage branch of each FET now exhibits a lower current level than the main branch of the opposite polarity FET.

In order to investigate the impact of Φ_{WF} on V_{th}, a number of FETs with Pd and Al gates were fabricated and then V_{th} of the n-branch ($V_{th\text{-}n}$) compared, as shown in Fig. 3.4.3. For the same t_{ox}, devices with Pd gate (Φ_{WF} ~5.1eV) show larger $V_{th\text{-}n}$ than the Al gated FETs (Φ_{WF} ~3.8eV). The impact of Φ_{WF} on V_{th} is about 600mV/eV. The V_{th} change as a function of Φ_{WF} exhibits a slope smaller than 1, which is not due to surface state pining. It is believed that one-dimensional systems do not suffer from this effect [3]. The non-ideal change of V_{th} with Φ_{WF} is attributed to the impact of oxide trapped charges and/or uncertainties in determining Φ_{WF}. Comparing samples with different t_{ox}, thicker oxides lead to larger $V_{th\text{-}n}$ as expected. Note, that $dV_{th\text{-}n}/d\Phi_{WF}$ is independent of t_{ox}. The wider band for thicker gate oxides is indicative of a larger error bar, potentially due to a larger amount of trapped charges.

Figure 3.4.4 shows the simulated V_{th} as a function of t_{ox}. Ideally, without the impact of oxide charges, a decrease of V_{th} by 120mV is expected when scaling t_{ox} from 20nm to 10nm.

The characteristics shown in Fig. 3.4.2 are measured for individual FETs with the source grounded. In an inverter set-up, the source voltages for the two FETs are associated with V_{dd}, hence, the two sets of characteristics need to be relatively shifted towards each other by V_{dd}. Figure 3.4.5, shows the shifted characteristics for three different V_{dd}. All of them possess a p-branch with an on-state higher than the off-state of the n-branch and vice versa – an indication of the successful implementation of the gate work function scheme. Besides the metal gate control on V_{th}, the structure also allows control of the electrostatics in both FETs simultaneously through a Si back gate. In Fig. 3.4.6, V_{th} is shown as a function of the Si gate voltage for both p- and n- branches: for 100nm SiO_2, V_{th} can be shifted by 1.5V with a supply voltage of -40V on Si. The electrostatic changes in the p- and n-branches are similar, as expected. With the well controlled V_{th} in both branches, a CMOS type inverter is formed on the same CN without introduction of chemical doping. The characteristics are shown in the right panel of Fig. 3.4.6 as a function of the Si gate voltage.

Finally, a circuit application is shown using the Φ_{WF} control on the V_{th} of the CNFET. A CMOS type, 5-stage ring oscillator (RO) is fabricated on an individual semiconducting CN [4]. The inset of Fig. 3.4.7 shows a SEM image of the RO. The device layout is the same as described in the context of Fig. 3.4.2. Interconnects between inverter stages are formed in the same lithographical process with the Pd gate. There are in total 6 inverters in the circuit: 5 are used for the RO while the last one functions as a read-out stage to prevent interference from the measurement set-up. A spectrum analyzer is used to record the Fourier transform of the oscillation as a function of V_{dd}. At V_{dd}=0.56V, the RO oscillates at 18MHz, and the frequency increases to 72MHz at V_{dd}=1.04V with a corresponding stage delay time of 1.4ns. The increased frequency is a result of the current increase through the FETs with increasing V_{dd}. The frequency response is consistent with the measured current (~μA) and the estimate for the parasitics in the circuit layout (~11fF). The small signal (few tens of μV to few hundred μV) is due to the mismatch between the MΩ output impedance of the circuit and the 50Ω input impedance of the spectrum analyzer. The use of an oscilloscope in high impedance would not provide good results either due to the limited driving current available from the CN output buffer to charge the input capacitance of the measuring instrument. The switching energy is calculated for all six inverters to be around 6.3fJ at V_{dd}=1.04V.

THz switching speed has been predicted for CNFETs based on a wrap-around device geometry with near zero SB line up at the contact interface [5]. Choosing the right CN diameter and S/D metal to ensure high current and sufficient on/off ratio is important for the circuit performance. Another crucial factor to increase the frequency is to decrease the parasitic capacitances in the circuit layout. In order to achieve THz performance, parasitics as low as a few tens of aF are needed for individual CNFETs carrying ~μA currents.

References:

[1] Z. Chen, et al., "The Role of Metal-Nanotube Contact in the Performance of Carbon Nanotube Field-Effect Transistors," *Nano Letters,* vol. 5, pp. 1497-1502, 2005.

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[4] Z. Chen, et al., "An Integrated Logic Circuit Assembled on a Single Carbon Nanotube," *Science,* vol. 311, pp. 1735, 2006.

[5] L.C. Castro and D.L. Pulfrey, "Method for Predicting fT for Carbon Nanotube FETs," *IEEE Trans. Nanotechnology,* vol. 4, pp. 699-704, 2005.

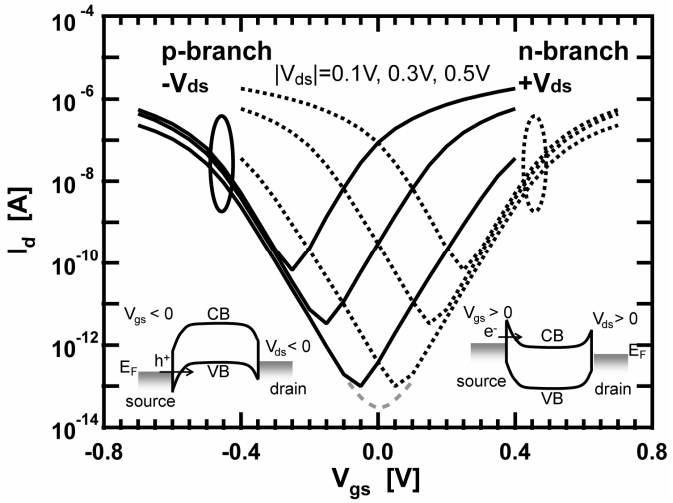

Figure 3.4.1: Simulated characteristics for a CNFET.

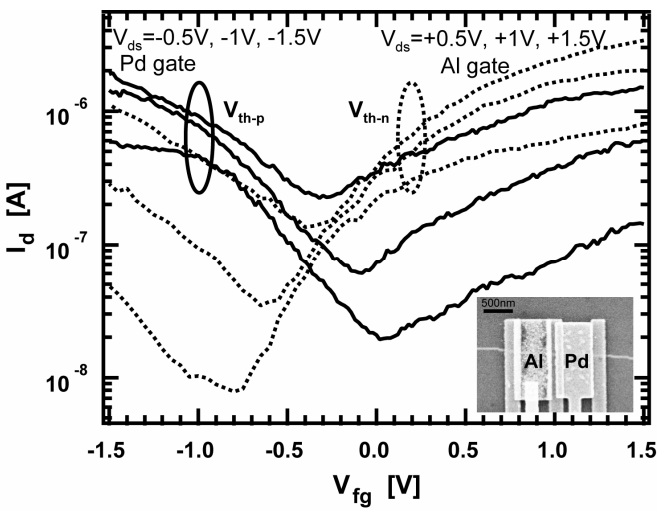

Figure 3.4.2: Subthreshold characteristics for a Pd-gated (solid lines) and an Al-gated (dashed lines) FET.

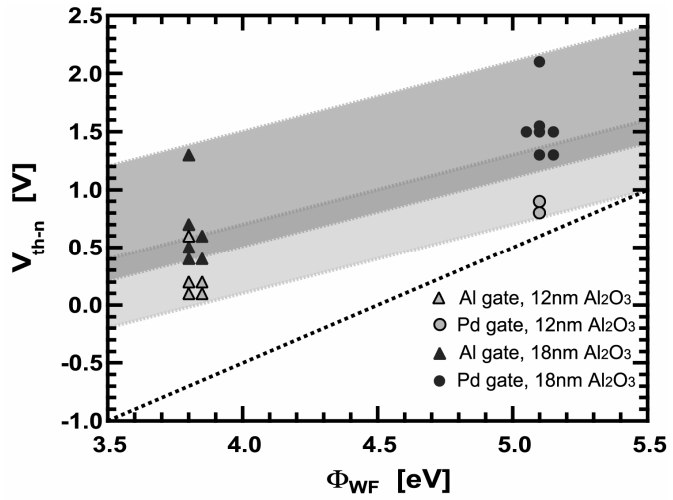

Figure 3.4.3: Threshold voltages of the n-branch from devices with Pd and Al metal gates and two different t_{ox}.

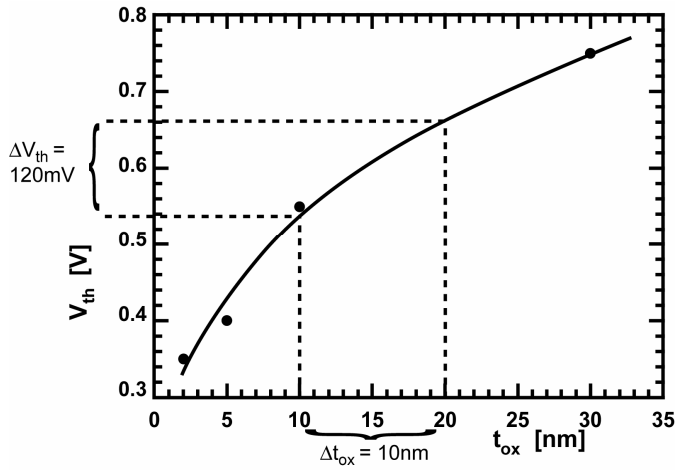

Figure 3.4.4: Simulated V_{th} as a function of t_{ox}, assuming an ideal oxide and a midgap line-up.

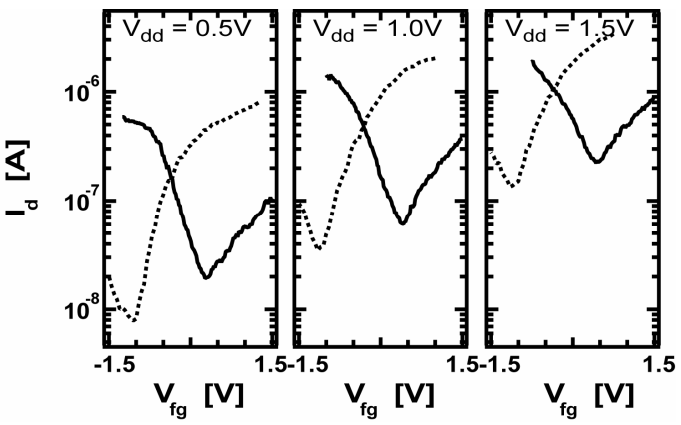

Figure 3.4.5: Characteristics for FETs in an inverter layout at different V_{dd} .

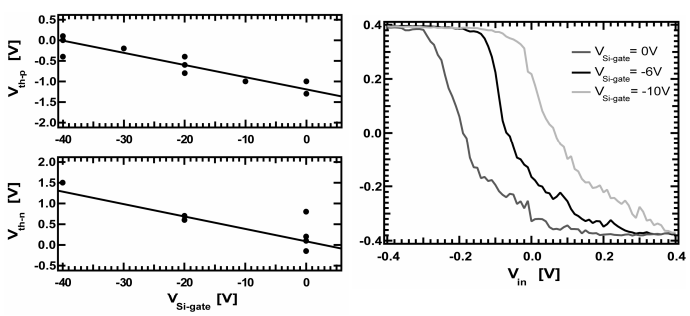

Figure 3.4.6: V_{th} (left) and inverter characteristics (right) as a function of the Si gate voltage.

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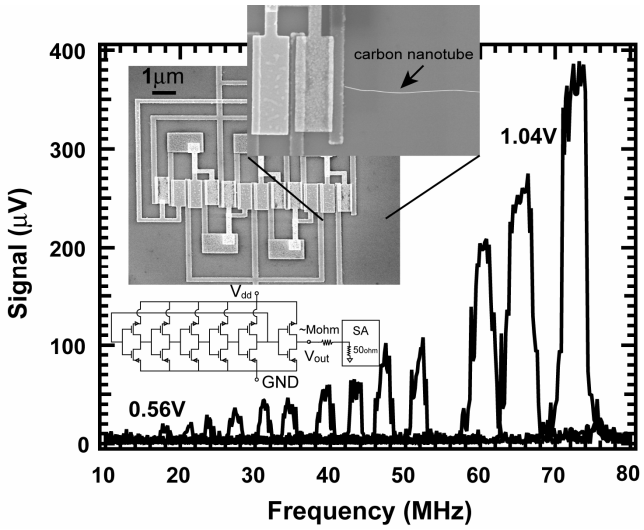

Figure 3.4.7: Frequency spectrum for a CN RO as a function of the supply voltage, V_{dd} =0.56V, 0.60V, … ,1.04V.

